What we claim as our invention is:

CLAIMS

[c1] 1. An apparatus to determine a transform of a block of encoded data, the block of encoded data comprising a plurality of data elements, the apparatus comprising:

an input register configured to receive a predetermined quantity of data elements;

at least one butterfly processor coupled to the input register, the butterfly processor configured to perform at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

at least one intermediate register coupled to the butterfly processor, the intermediate register configured to temporarily store the processed data; and

a feedback loop coupling the intermediate register and the butterfly processor, where if enabled, is configured to transfer a first portion of processed data elements to the appropriate butterfly processor to perform additional mathematical operations and, where if disabled, is configured to transfer a second portion of processed data elements to at least one holding register;

wherein the holding register is configured to store the processed data until all of the first portion data elements is processed.

[c2] 2. The apparatus set forth in Claim 1, further comprising at least one input multiplexer coupling the feedback loop and the intermediate register, wherein each input multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate butterfly processor.

[c3] 3. The apparatus set forth in Claim 1, further comprising at least one output multiplexer coupling the butterfly processor and the intermediate register, wherein each output multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate intermediate register.

[c4] 4. The apparatus set forth in Claim 1, wherein the transform is selected from the group consisting of: a Discrete Cosine Transform (DCT), a Differential Quadtree Transform (DQT), an Inverse Discrete Cosine Transform (IDCT) and an Inverse Differential Quadtree Transform (IDQT).

[c5] 5. The apparatus set forth in Claim 1 wherein the block of encoded data may be represented as row data and column data, and further comprising a transpose random-access memory (RAM) coupled to the input register, wherein the transpose RAM is configured to store the row data while the column data is being processed, and wherein the transpose RAM is configured to store the column data while the row data is being processed.

[c6] 6. The apparatus set forth in Claim 5, wherein the transpose RAM is configurable to store two blocks of encoded data.

[c7] 7. The apparatus set forth in Claim 5, further comprising a write multiplexer coupling the holding register, wherein the write multiplexer is configured to resequence data elements to complete a one-dimensional transform.

[c8] 8. The apparatus set forth in Claim 1 wherein the feedback loop allows for the same components to be reused irrespective of block size.

[c9] 9. The apparatus set forth in Claim 1 wherein the feedback loop allows for the same components to be reused irrespective of the type of transform.

[c10] 10. The apparatus set forth in Claim 1 wherein the feedback loop allows for the same components to be reused irrespective of mathematical operation.

[c11] 11. The apparatus set forth in Claim 1, further comprising a control sequencer coupled to the feedback loop, wherein the control sequencer is configured to enable or disable the feedback loop.

[c12] 12. The apparatus set forth in Claim 11, where the control sequencer provides the butterfly processor with a unique coefficient multiplier.

[c13] 13. The apparatus set forth in Claim 12, wherein the unique coefficient multiplier is based on B.G. Lee's algorithm.

[c14] 14. The apparatus set forth in Claim 11, where the control sequencer enables certain ones of the input registers based on a predetermined event.

[c15] 15. The apparatus set forth in Claim 11, where the control sequencer enables certain ones of the butterfly processors based on predetermined criteria.

[c16] 16. The apparatus set forth in Claim 11, where the control sequencer enables certain ones of the intermediate registers based on predetermined criteria.

[c17] 17. The apparatus set forth in Claim 11, where the control sequencer enables certain ones of the output registers based on predetermined criteria.

[c18] 18. The apparatus as set forth in Claim 1, wherein the mathematical operation is from the group consisting of addition, multiplication, and subtraction.

[c19] 19. The apparatus as set forth in Claim 1, wherein each butterfly processor performs a portion of a one-dimensional transform.

[c20] 20. The apparatus as set forth in Claim 1, wherein the transform of a block of encoded data is computed as a series of one-dimensional transforms.

[c21] 21. An apparatus to determine a transform of a block of encoded data, the block of encoded data capable of being represented as row data and column data, each row and column comprising a plurality of data elements, the apparatus comprising:

a transpose random access memory (RAM) configured to store the block of encoded data;

at least one input register coupled to the transpose RAM, the input register configured to receive columns of data from the transpose RAM;

at least one butterfly processor coupled to the input register, the butterfly processor configured to perform a portion of a one-dimensional transform on selected pairs of data elements from the column data to produce an output of first order column data;

at least one intermediate register coupled to the butterfly processor, the intermediate register configured to temporarily store the first order column data; and

a feedback loop coupling the intermediate register and the butterfly processor, where if enabled, is configured to transfer selected data elements of the first order column data to the butterfly processor to perform additional portions of one-dimensional transforms and, where if disabled, is configured to transfer the column data to the transpose RAM;

wherein the input register is then configured to receive rows of data from the transpose RAM, the butterfly processor is configured to perform a portion of a one dimensional transform on selected pairs of data elements from the rows of data to produce an output of first order row data, the intermediate register configured to temporarily store the first order row data, the feedback loop configured to transfer selected data elements of the first order row data to the butterfly processor to perform additional portions of one-dimensional transforms and, where if disabled, is configured to transfer the row data to an output register.

[c22] 22. The apparatus as set forth in Claim 21, wherein the feedback loop is disabled upon completing a one-dimensional transform on the column or row data.

[c23] 23. The apparatus set forth in Claim 21, further comprising at least one input multiplexer coupling the feedback loop and the intermediate register, wherein each input multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate butterfly processor.

[c24] 24. The apparatus set forth in Claim 21, further comprising at least one output multiplexer coupling the butterfly processor and the intermediate register, wherein each output multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate intermediate register.

[c25] 25. The apparatus set forth in Claim 21, wherein the transform is selected from the group consisting of: a Discrete Cosine Transform (DCT), a Differential Quadtree Transform (DQT), an Inverse Discrete Cosine Transform (IDCT) and an Inverse Differential Quadtree Transform (IDQT).

[c26] 26. The apparatus set forth in Claim 21, wherein the transpose RAM is configurable to store two blocks of encoded data.

[c27] 27. The apparatus set forth in Claim 21, further comprising a write multiplexer coupling the holding register, wherein the write multiplexer is configured to resequence data elements such that the one-dimensional transform is completed.

[c28] 28. The apparatus set forth in Claim 21 wherein the feedback loop allows for the same components to be reused irrespective of block size, type of transform or type of mathematical operation.

[c29] 29. The apparatus set forth in Claim 21, further comprising a control sequencer coupled to the feedback loop, wherein the control sequencer is configured to enable or disable the feedback loop.

[c30] 30. The apparatus set forth in Claim 29, where the control sequencer provides the butterfly processor with a unique coefficient multiplier.

[c31] 31. The apparatus set forth in Claim 29, wherein the unique coefficient multiplier is based on B.G. Lee's algorithm.

[c32] 32. The apparatus set forth in Claim 29, where the control sequencer enables certain ones of the input registers, butterfly processors, intermediate registers, or output registers based on predetermined criteria.

[c33] 33. The apparatus as set forth in Claim 21, wherein the mathematical operation is from the group consisting of addition, multiplication, and subtraction.

[c34] 34. The apparatus as set forth in Claim 21, wherein each butterfly processor performs a portion of a one-dimensional transform.

[c35] 35. The apparatus as set forth in Claim 21, wherein the transform of a block of encoded data is computed as a series of one-dimensional transforms.

[c36] 36. An apparatus to perform an N dimensional transform as a cascade of N one-dimensional transforms on a block of encoded data, the encoded data comprising a plurality of data elements, the apparatus comprising:

a cluster of butterfly processors coupled to the input register, each butterfly processor configured to perform a portion of a one-dimensional transform on selected pairs of data elements to produce an output of partially processed data comprising a plurality of partially processed data elements;

at least one intermediate register coupled to each butterfly processor, the intermediate register configured to temporarily store the partially processed data; and

a feedback loop coupled to the intermediate register and the butterfly processor, where the feedback loop is enabled as necessary to route selected pairs of the partially processed data elements to the appropriate butterfly processor to perform additional portions of one-dimensional transforms until a one dimensional transform is completed.

[c37] 37. The apparatus set forth in Claim 36, wherein the transform is selected from the group consisting of: a Discrete Cosine Transform (DCT), a Differential Quadtree Transform (DQT), an Inverse Discrete Cosine Transform (IDCT) and an Inverse Differential Quadtree Transform (IDQT).

[c38] 38. The apparatus set forth in Claim 36 wherein the block of encoded data may be represented as row data and column data, and further comprising a transpose read-only memory (RAM) coupled to the input register, wherein the transpose RAM is configured to store the row data while the column data is being processed, and wherein the transpose RAM is configured to store the column data while the row data is being processed.

[c39] 39. The apparatus set forth in Claim 38, wherein the transpose RAM is configurable to store two blocks of encoded data.

[c40] 40. The apparatus set forth in Claim 36 wherein the feedback loop allows for the same components to be reused irrespective of block size, type of transform or type of mathematical operation.

[c41] 41. The apparatus set forth in Claim 36, further comprising a control sequencer coupled to the feedback loop, wherein the control sequencer is configured to enable or disable the feedback loop.

[c42] 42. The apparatus set forth in Claim 41, where the control sequencer provides the butterfly processor with a unique coefficient multiplier.

[c43] 43. The apparatus set forth in Claim 42, wherein the unique coefficient multiplier is based on B.G. Lee's algorithm.

[c44] 44. The apparatus set forth in Claim 41, where the control sequencer enables certain ones of the input registers, butterfly processors, intermediate registers, or output registers based on predetermined criteria.

[c45] 45. An apparatus to determine the inverse discrete cosine transform of a block of encoded data, the block of encoded data comprising a plurality of data elements, the apparatus comprising:

an input register configured to receive a predetermined quantity of data elements;

at least one butterfly processor coupled to the input register, the butterfly processor configured to perform at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

at least one intermediate register coupled to the butterfly processor, the intermediate register configured to temporarily store the processed data; and

a feedback loop coupling the intermediate register and the butterfly processor, where if enabled, is configured to transfer a first portion of processed data elements to the appropriate butterfly processor to perform additional mathematical operations and, where if disabled, is configured to transfer a second portion of processed data elements to at least one holding register;

wherein the holding register is configured to store the processed data until all of the first portion data elements is processed.

[c46] 46. An apparatus to determine a transform of a block of encoded data, the block of encoded data capable of being represented as row data and column data, each row and column comprising a plurality of data elements, the apparatus comprising:

a transpose random-access memory (RAM) configured to store the block of encoded data;

at least one input register coupled to the transpose RAM, the input register configured to receive columns of data from the transpose RAM;

at least one butterfly processor coupled to the input register, the butterfly processor configured to perform a first order transform on selected pairs of data elements from the column data to produce an output of first order column data;

at least one intermediate register coupled to the butterfly processor, the intermediate register configured to temporarily store the first order column data;

a feedback loop coupling the intermediate register and the butterfly processor, where if enabled, is configured to transfer selected data elements of the first order column data to the butterfly processor to perform additional transforms and, where if disabled, is configured to transfer the column data to the transpose RAM; and

a control sequencer coupled to the feedback loop, wherein the control sequencer is configured to enable or disable the feedback loop

wherein the input register is then configured to receive rows of data from the transpose RAM, the butterfly processor is configured to perform a first order transform on selected pairs of data elements from the rows of data to produce an output of first order row data, the intermediate register is configured to temporarily store the first order row data, the feedback loop is configured to transfer selected data elements of the first order row data to the butterfly processor to perform additional transforms and, where if disabled, is configured to transfer the row data to an output register.

[c47] 47. A method to determine a transform of a block of encoded data, the block of encoded data comprising a plurality of data elements, the method comprising:

(a) receiving a predetermined quantity of data elements;

(b) performing at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

(c) making a determination as to whether any of the processed data elements require additional mathematical operations;

(d) selecting a first portion of processed data elements that require additional mathematical operations;

(e) selecting a second portion of processed data elements that do not require additional mathematical operations;

(f) performing at least one mathematical operation on selected pairs of the first portion of processed data elements to produce a second output of processed data elements; and

(g) storing the second portion of processed data elements until all of the first portion of data elements is processed.

[c48] 48. The method set forth in Claim 47, further comprising:

(h) repeating steps (c), (d), (e), (f) and (g) as necessary.

[c49] 49. The method set forth in Claim 47, further comprising:

(i) outputting the block of encoded data when all of the data elements of the block of encoded data do not require additional mathematical operations.

[c50] 50. The method set forth in Claim 47, wherein the transform is selected from the group consisting of: a Discrete Cosine Transform (DCT), a Differential Quadtree Transform (DQT), an Inverse Discrete Cosine Transform (IDCT) and an Inverse Differential Quadtree Transform (IDQT).

[c51] 51. The method set forth in Claim 47 wherein the block of encoded data may be represented as row data and column data, and further comprising:

storing the row data while the column data is being processed; and

storing the column data while the row data is being processed.

[c52] 52. The method set forth in Claim 47, further comprising resequencing data elements before the step of storing, such that subsequent delivery of data elements is performed in an efficient manner.

[c53] 53. The method set forth in Claim 47, further comprising controlling steps (a), (b), (c), (d), (e), (f), (g), and (h) based upon predetermined criteria.

[c54] 54. The method set forth in Claim 53, further comprising providing a unique coefficient multiplier to certain data elements based upon predetermined criteria.

[c55] 55. The apparatus set forth in Claim 54, wherein the unique coefficient multiplier is based on B.G. Lee's algorithm.

[c56] 56. The method set forth in Claim 47, wherein the mathematical operation is from the group consisting of addition, multiplication, and subtraction.

[c57] 57. The method as set forth in Claim 47, wherein each butterfly processor performs a portion of a one-dimensional transform.

[c58] 58. The method as set forth in Claim 47, wherein the transform of a block of encoded data is computed as a series of one-dimensional transforms.

[c59] 59. A computer readable medium containing constructions for controlling a computer system to perform a method, the method comprising:

(a) receiving a predetermined quantity of data elements;

(b) performing at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

(c) making a determination as to whether any of the processed data elements require additional mathematical operations;

(d) selecting a first portion of processed data elements that require additional mathematical operations;

(e) selecting a second portion of processed data elements that do not require additional mathematical operations;

(f) performing at least one mathematical operation on selected pairs of the first portion of processed data elements to produce a second output of processed data elements; and

(g) storing the second portion of processed data elements until all of the first portion of data elements is processed.

[c60] 60. An apparatus to determine a transform of a block of encoded data, the block of encoded data comprising a plurality of data elements, the apparatus comprising:

(a) means for receiving a predetermined quantity of data elements;

(b) means for performing at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

(c) means for making a determination as to whether any of the processed data elements require additional mathematical operations;

(d) means for selecting a first portion of processed data elements that require additional mathematical operations;

(e) means for selecting a second portion of processed data elements that do not require additional mathematical operations;

(f) means for performing at least one mathematical operation on selected pairs of the first portion of processed data elements to produce a second output of processed data elements; and

(g) means for storing the second portion of processed data elements until all of the first portion of data elements is processed.

[c61] 61. The apparatus set forth in Claim 47, further comprising:

(h) means for repeating steps (c), (d), (e), (f) and (g) as necessary.

[c62] 62. The apparatus set forth in Claim 47, further comprising:

(i) means for outputting the block of encoded data when all of the data elements of the block of encoded data do not require additional mathematical operations.

[c63] 63. The apparatus set forth in Claim 47, wherein the transform is selected from the group consisting of: a Discrete Cosine Transform (DCT), a Differential

Quadtree Transform (DQT), an Inverse Discrete Cosine Transform (IDCT) and an Inverse Differential Quadtree Transform (IDQT).

[c64] 64. The apparatus set forth in Claim 47 wherein the block of encoded data may be represented as row data and column data, and further comprising:

means for storing the row data while the column data is being processed; and

means for storing the column data while the row data is being processed.

[c65] 65. The apparatus set forth in Claim 47, further comprising means for resequencing data elements before the step of storing, such that subsequent delivery of data elements is performed in an efficient manner.

[c66] 66. The apparatus set forth in Claim 47, further comprising means for controlling elements (a), (b), (c), (d), (e), (f), (g), and (h) based upon predetermined criteria.

[c67] 67. The apparatus set forth in Claim 66, further comprising providing a unique coefficient multiplier to certain data elements based upon predetermined criteria.

[c68] 68. The apparatus set forth in Claim 67, wherein the unique coefficient multiplier is based on B.G. Lee's algorithm.

[c69] 69. The apparatus set forth in Claim 60, wherein the mathematical operation is from the group consisting of addition, multiplication, and subtraction.

[c70] 70. The apparatus as set forth in Claim 60, wherein each butterfly processor performs a portion of a one-dimensional transform.

[c71] 71. An apparatus to determine a transform of encoded data, the encoded data comprising a plurality of data elements in the pixel domain, the apparatus comprising:

a block size assigner configured to receive the plurality of data elements and group the elements into a plurality of groups of data elements in the pixel domain;

a DCT/DQT transformer configured to transform the data elements from the pixel domain to the frequency domain, the transformer further comprising:

an input register configured to receive a predetermined quantity of data elements of the group;

at least one butterfly processor coupled to the input register, the butterfly processor configured to perform at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

at least one intermediate register coupled to the butterfly processor, the intermediate register configured to temporarily store the processed data; and

a feedback loop coupling the intermediate register and the butterfly processor, where if enabled, is configured to transfer a first portion of processed data elements to the appropriate butterfly processor to perform additional mathematical operations and, where if disabled, is configured to transfer a second portion of processed data elements to at least one holding register;

wherein the holding register is configured to store the processed data until all of the first portion data elements is processed;

a quantizer configured to quantize the frequency domain elements to emphasize those elements that are more sensitive to the human visual system, and de-emphasize those elements that are less sensitive to the human visual system;

a serializer configured to produce a serialized stream of frequency domain elements; and

a variable length coder configured to determine successive frequency domain elements and non-successive frequency domain elements.

[c72] 72. The apparatus set forth in Claim 71, further comprising at least one input multiplexer coupling the feedback loop and the intermediate register, wherein each input multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate butterfly processor.

[c73] 73. The apparatus set forth in Claim 71, further comprising at least one output multiplexer coupling the butterfly processor and the intermediate register, wherein each output multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate intermediate register.

[c74] 74. The apparatus set forth in Claim 71 wherein the block of encoded data may be represented as row data and column data, and further comprising a transpose random-access memory (RAM) coupled to the input register, wherein the transpose RAM is configured to store the row data while the column data is being processed, and wherein the transpose RAM is configured to store the column data while the row data is being processed.

[c75] 75. The apparatus set forth in Claim 74, wherein the transpose RAM is configurable to store two blocks of encoded data.

[c76] 76. The apparatus set forth in Claim 74, further comprising a write multiplexer coupling the holding register, wherein the write multiplexer is configured to resequence data elements to complete a one-dimensional transform.

[c77] 77. The apparatus set forth in Claim 71 wherein the feedback loop allows for the same components to be reused irrespective of block size.

[c78] 78. The apparatus set forth in Claim 71, further comprising a control sequencer coupled to the feedback loop, wherein the control sequencer is configured to enable or disable the feedback loop.

[c79] 79. The apparatus set forth in Claim 78, where the control sequencer provides the butterfly processor with a unique coefficient multiplier.

[c80] 80. The apparatus set forth in Claim 78, where the control sequencer enables certain ones of the input registers based on a predetermined event.

[c81] 81. The apparatus set forth in Claim 78, where the control sequencer enables certain ones of the butterfly processors based on predetermined criteria.

[c82] 82. The apparatus set forth in Claim 78, where the control sequencer enables certain ones of the intermediate registers based on predetermined criteria.

[c83] 83. The apparatus set forth in Claim 78, where the control sequencer enables certain ones of the output registers based on predetermined criteria.

[c84] 84. The apparatus as set forth in Claim 71, wherein the mathematical operation is from the group consisting of addition, multiplication, and subtraction.

[c85] 85. The apparatus as set forth in Claim 71, wherein each butterfly processor performs a portion of a one-dimensional transform.

[c86] 86. A method of transforming encoded data from the pixel domain to the frequency domain, the encoded data comprising a plurality of data elements, the method comprising:

(a) grouping the plurality of data elements in the pixel domain into a plurality of blocks, each block comprising a plurality of data elements in the pixel domain;

(b) performing at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

(c) making a determination as to whether any of the processed data elements require additional mathematical operations;

(d) selecting a first portion of processed data elements that require additional mathematical operations;

(e) selecting a second portion of processed data elements that do not require additional mathematical operations;

(f) performing at least one mathematical operation on selected pairs of the first portion of processed data elements to produce a second output of processed data elements;

(g) storing the second portion of processed data elements until all of the first portion of data elements is processed;

(h) repeating steps (c), (d), (e), (f) and (g), as necessary, until all of the data elements do not require additional mathematical operations and are converted to frequency domain elements;

(i) quantizing the frequency domain data elements to emphasize those elements that are more sensitive to the human visual system and de-emphasize those elements that are less sensitive to the human visual system;

(j) serializing the quantized frequency domain data elements to produce a serialized stream of frequency domain elements; and

(k) coding the serialized frequency domain elements to determine successive frequency domain elements and non-successive frequency domain elements.

[c87] 87. The method set forth in Claim 86 wherein the block of encoded data may be represented as row data and column data, and further comprising:

storing the row data while the column data is being processed; and

storing the column data while the row data is being processed.

[c88] 88. The method set forth in Claim 86, further comprising controlling steps (a), (b), (c), (d), (e), (f), (g), and (h) based upon required control signals.

[c89] 89. The method set forth in Claim 88, further comprising providing a unique coefficient multiplier to certain data elements based upon predetermined criteria.

[c90] 90. The method as set forth in Claim 86, wherein each butterfly processor performs a portion of a one-dimensional transform.

[c91] 91. The method as set forth in Claim 86, wherein the transform of a block of encoded data is computed as a series of one-dimensional transforms.